A NEW CMOS DESIGN AND ANALYSIS OF CURRENT CONVEYOR SECOND GENERATION (CCII)

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Abstract

This paper describes the current conveyors used as a basic building block in a variety of electronic circuit in instrumentation and communication systems. Today these systems are replacing the conventional Op-amp in so many applications such as active filters, analog signal processing. Current conveyors are unity gain active building block having high linearity, wide dynamic range and provide higher gain bandwidth

The proposed current conveyors are simulated using TSMC 0.18μm CMOS technology on Advanced Design System and the results are also tabulated for comparison. The main features of these current conveyors are low voltage, less power, high slew rate and wide bandwidth for voltage transfer (V_y to V_x) and current transfer (I_x to I_z) which make them suitable for high frequency and low power applications.

Keywords

Bulk-Driven transistors, Current Conveyor ofSecond Generation CCII, CMOS integrated circuit, PSPICE simulation.

1. INTRODUCTION

One of the most basic building blocks in the area of current-mode analogue signal processing is the current conveyor (CC).The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [1]. CCI was then replaced by a more versatile second-generation device in 1970 [2], the CCII. Current conveyor designshave mainly been with BJTs due to their high transconductance values compared to their CMOS counterparts. They are used as current-feedback operational amplifiers like the MAX477 high-speed amplifier and the MAX4112 low-power amplifier, which both feature current feedback rather than the conventional voltage feedback used by standard operational amplifiers. Current conveyors are used in high-frequency applications where the conventional operational amplifiers cannot be used, because the conventional designs are limited by their gain-bandwidth product.

The current mode circuits such as Current conveyors (CCs) have received considerable attention and emerged as an alternate building block to the Op-Amp (voltage mode circuit) in the field of analog signal processing [3] due to its potential performance feature. In CCs, the use of current rather than voltage as the active parameter can result in a higher usable gain, accuracy and bandwidth due to reduced voltage excursion at sensitive nodes [4]. The current conveyors are not only useful for current processing, but also offer certain important advantages in voltage processing circuits. The nonlinear circuits and dynamics [5] can easily be developed using CCs.

With the reduction in the supply voltage and device threshold voltage of CMOS technology, the performance of CMOS voltage mode circuits has greatly affected which results in a reduced dynamic range, an increased propagation delay and reduced noise margins. The CCs have simple structure, wide bandwidth and capability to operate at low voltage. It also offer unity current gain, unity voltage gain, higher linearity, wider dynamic range and better high frequency performance.

2. THE CURRENT CONVEYOR CC

The current conveyor is functionally flexible and versatile in nature as it has precise unity voltage gain between X and Y; unity current gain between Z and X as shown inFig. 1, rather than the high ill-defined open loop gain of Op-Amps. Because of this fact, CCII is generally used without feedback in amplifier applications [6, 7].
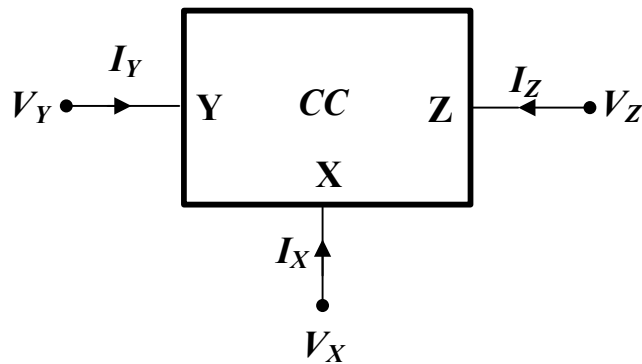

Fig. 1: Building block of Current conveyor

The build block of current conveyor and its generalised characteristics equation are represented by the following hybrid matrix.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ b & 0 & 0 \\ 0 & c & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

The current conveyor is a grounded three-port network represented by the black box (Fig 1) with the three ports denoted by X, Y, and Z. Its terminal characteristics can be represented best by a hybrid matrix giving the outputs of the three ports in terms of their corresponding inputs [8].

3. CURRENT CONVEYOR SECOND GENERATION CCII

The second-generation current conveyor (CCII) is used as a basic building block in many current-mode analog circuits. It offers high input impedance at voltage input port Y, which is preferable in order to avoid loading effect. So, second generation current conveyor is developed to overcome the problem loading effect of CCI. The CCII is considered as a basic building block in analog circuit design because all the analog applications can be developed by making suitable connections of one or more CCIIs with passive and active components.

The second-generation current conveyor is a grounded three-terminal (X, Y and Z) device as shown in Fig. 2 (a), and the equivalent circuit of the ideal CCII is shown in Fig. 2 (b).
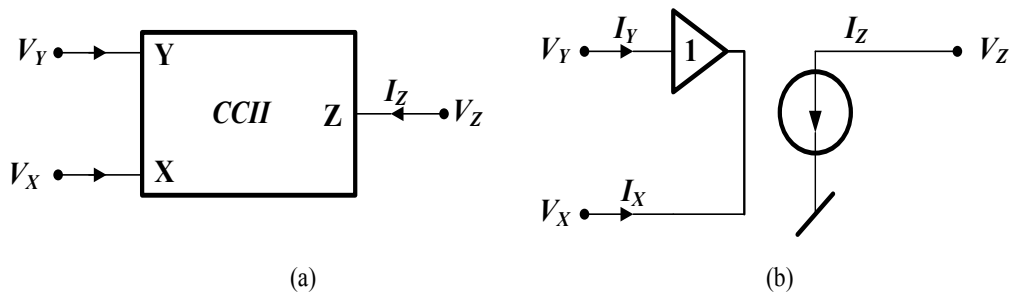

(a)   (b)

Fig. 2: (a) The CCII symbol, (b) ideal equivalent circuit.

The characteristics of ideal CCII are represented by the following hybrid matrix

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (2)$$

An ideal CCII has the following characteristics:

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- Infinite input impedance at terminal Y ($R_Y = \infty$ and $I_Y = 0$)
- Zero input impedance at terminal X ($R_X = 0$)
- Accurate voltage copy from terminal Y to X ($V_X = V_Y$)
- Accurate current copy from terminal X to Z with infinite output impedance at Z ($I_Z = I_X$ and $R_Z = \infty$)

4. OPERATIONS USING THE IDEAL CCII

- **<u>Amplifiers using CCII</u>**

The CCII can easily be used to form the current output amplifiers and voltage-output amplifier as shown in Fig. 3.The voltage- and current- gains are as follows:

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} \quad (3)$$

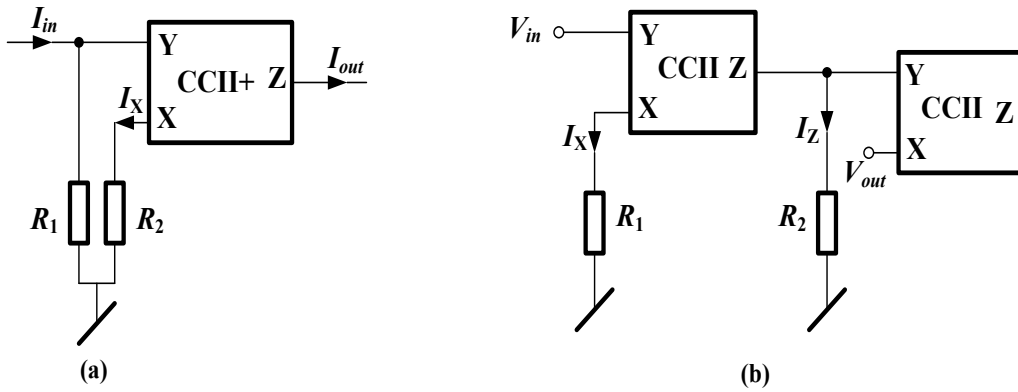$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1} \quad (4)$$

(a)   (b)

Fig. 3: (a) CCII-based current amplifier, (b) CCII-based voltage amplifier.

- **Integrators using CCII**

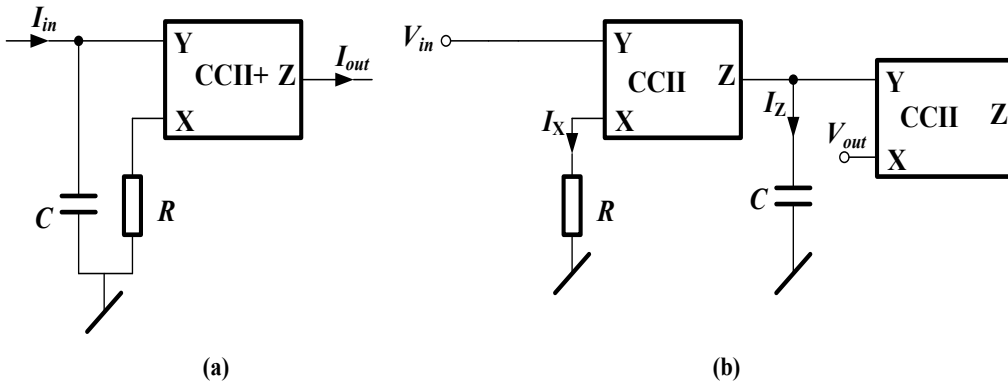In Fig. 4, simple current- and voltage- integrators are presented.

(a)   (b)

Fig. 4: (a) CCII-based current integrator, (b) CCII-based voltage integrator.

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The output signals are as follows:

$$I_{out} = \frac{I_{in}}{sCR} \qquad (5)$$

$$V_{out} = \frac{V_{in}}{sCR} \qquad (6)$$

- **Adders using CCII**

In Fig. 5, CCII-based current adder and CCII-based voltage adder are reported, with the following equations:

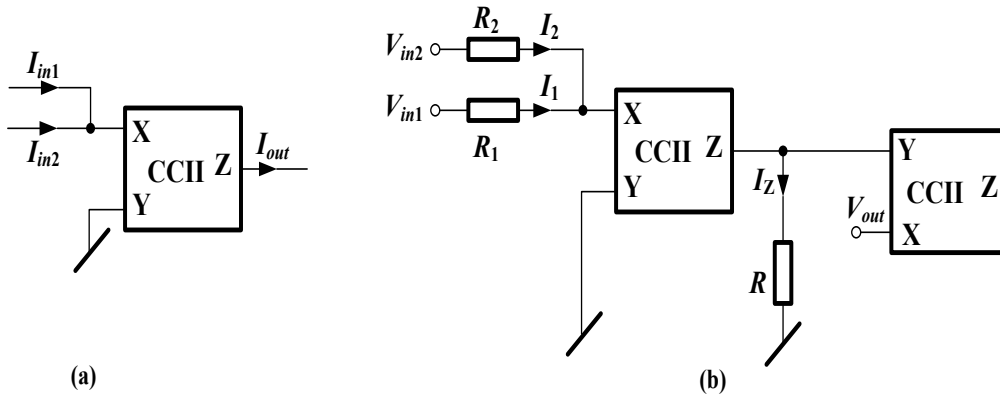(a)   (b)

Fig. 5: (a) CCII-based current adder, (b) CCII-based voltage adder.

$$I_{out} = -(I_{in1} + I_{in2}) \quad (7)$$

$$V_{out} = -\frac{R}{R_1}V_{in1} - \frac{R}{R_2}V_{ir} \qquad (8)$$

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- **Differentiators using CCII**

Current- and voltage-mode versions are shown in Fig. 6. The output signals are as follows:
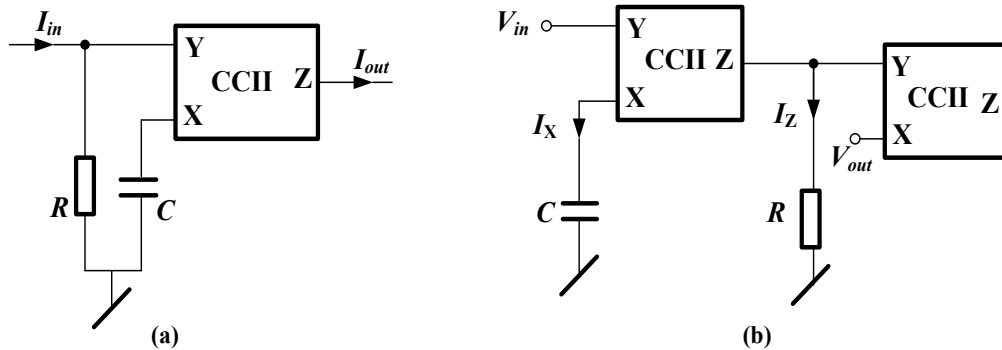

| (a) | (b) |

Fig. 6: (a) CCII-based current differentiator, (b) CCII-based voltage differentiator.

5. PROPOSED CMOS CURRENT CONVEYOR SECOND GENERATION

A new connection of Bulk-driven OTA is used to realize the CCII. In the OTA-based approach, presented in Fig.7, Bulk-driven OTA is used to implement the unity gain buffer between the Y and X inputs [9]. The X input current I_x is sensed by duplicating buffers, output transistors M_6 and M_7 using transistors M_8 and M_9, and extracting the X current from them as I_z. Since transistors M_8 and M_9 have the same size and gate-source voltage as the output stage transistors M_6 and M_7, the current I_z should be a copy of the current flowing through M_6 and M_7 which is I_x. Transistors M_{10}-$M_{15}$are used to generate I_z. Since no additional transistors need to be inserted between the OTA and rails, the approach will not increase the minimum operating voltage over that of the operational core. In addition the voltage follower is based on an OTA, thus it will maintain all the benefits and also the disadvantages of such a circuit i.e. a good voltage follower at the cost of lower bandwidth [10].
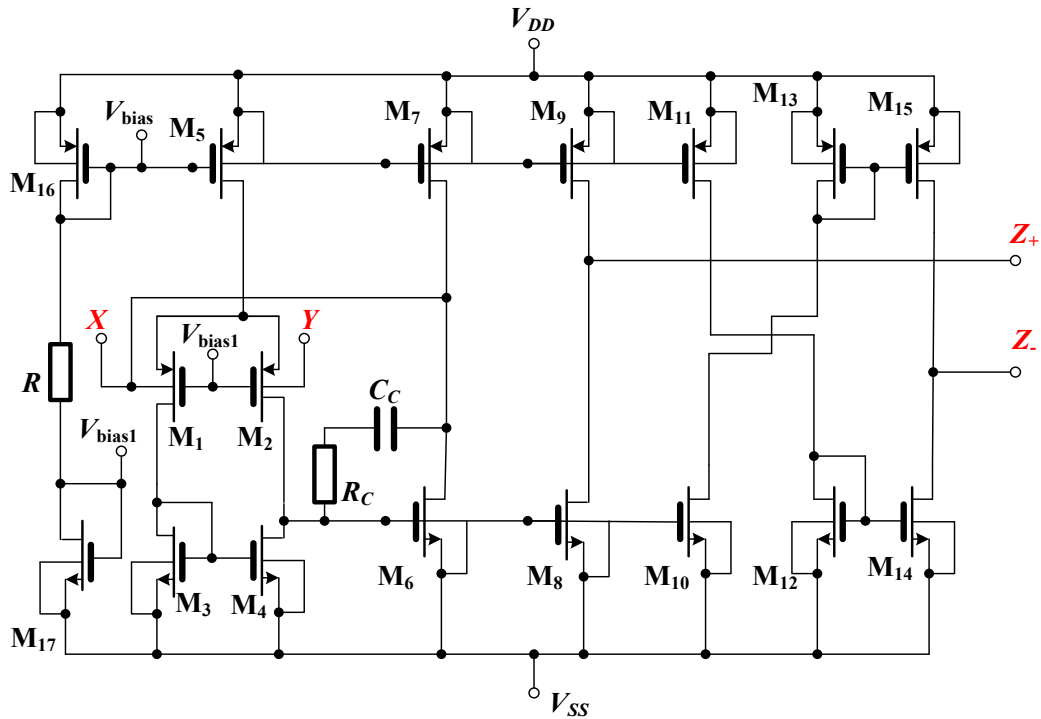
Fig. 7: Bulk-driven CCII± based on Bulk-driven OTA.

The aspect ratios of each of the transistors used the CCII in Fig. 7 are listed in Table1.

$V_{DD} \& V_{SS} = \pm 0.6$V, $R = 5$kΩ, $R_C = 4.7$kΩ, $C_C = 0.5$pF

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Transistor	Length (μm)	Width (μm)
M_1, M_2	2	30
M_3, M_4	2	4
M_5, M_{16}	3	20
$M_6, M_8, M_{10}, M_{12}, M_{14}$	2	16
$M_7, M_9, M_{11}, M_{13}, M_{15}$	3	40
M_{17}	3	10

Table 1. Aspect ratios of the transistors used in the CCII in Fig. 7.

6. SIMULATION RESULTS

The simulated frequency responses of current gains I_{z+}/I_x, I_{z-}/I_x are given in Fig. 8. The cut off frequencies for the gains are 20 MHz and 52 MHz, respectively.

In Fig. 9, the input voltage buffer behaviour is shown. A DC sweep simulation has been performed, to check the range in which the voltage on X node is equal to the voltage applied to Y node.

The current linearity between X and Y terminal of the bulk-driven current conveyor (CCII±) from Fig. 7, is demonstrated in Fig. 10. Note that for input currents I_x and I_z, the boundary of linear operation is ca±16μA. The corresponding small-signal current gains are as follows: I_{z+}/I_x, $I_{z-}/I_x = 1$, and the corresponding voltage gain $V_x/V_Y = 0.97$.

The small-signal low frequency resistance of the X terminal R_x is equal to 166Ω as shown in Fig. 11. The small-signal resistance of the Y terminal R_Y is equal to 50GΩ.

The small-low frequency signal resistances of the Z_+, Z_- outputs terminals are equal to 560kΩ, and 554kΩ, respectively. Simulation results of the CCII± are summarized in Table 2.
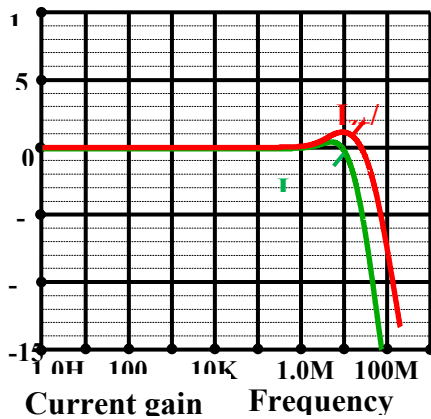

Fig. 8: Frequency variation of the current gains I_{z+}/I_x, I_z/I_x in dB of the CCII in Fig. 7.
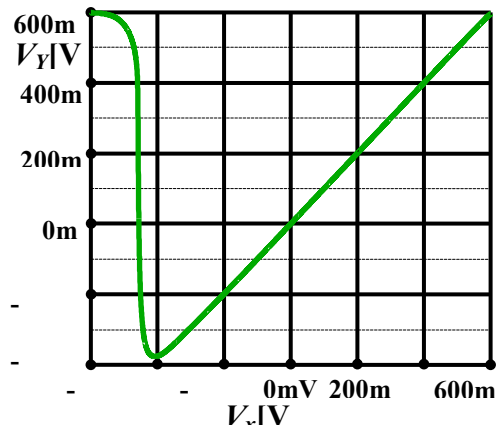
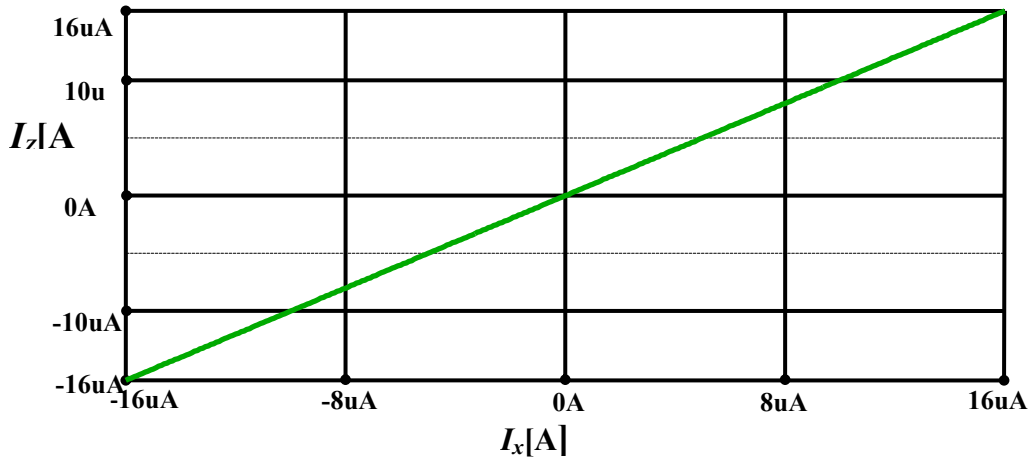**Fig. 9: Voltage follower between X and Y of the CCII in Fig. 7.**

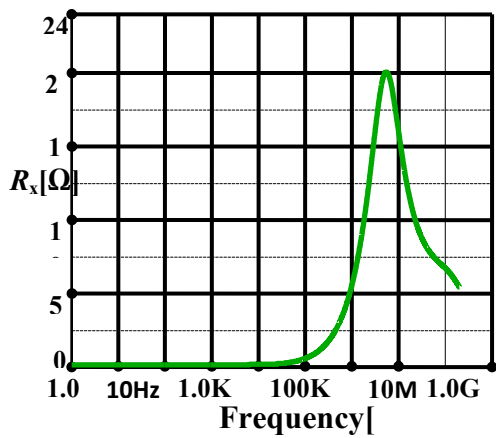**Fig. 10: Current linearity between X and Y of the CCII in Fig. 7**

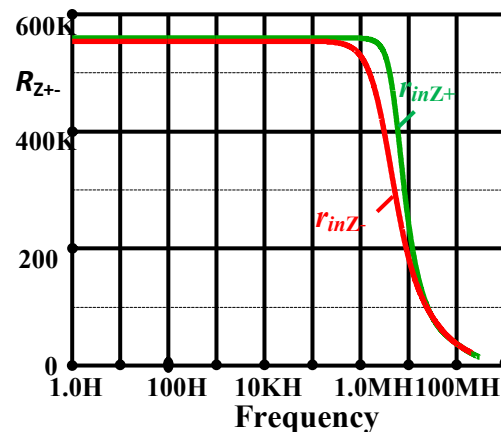**Fig. 11: The X node input resistance $r_{in,x}$ of the CCII in Fig. 7.**

Fig. 12: The Z node output resistance $r_{in,Z}$ of the CCII in Fig. 7.

Characteristics	Simulation Result
Power consumption	119 μW

3-dB bandwidth I_{Z+}/I_X	20 MHz
3-dB bandwidth I_{Z-}/I_X	52 MHz
DC voltage range	-400, 600 mV
DC current range	±16 µA
Current gain I_Z/I_X	1
Voltage gain V_X/V_Y	0.97
Node X parasitic DC resistance	166 Ω
Node Y parasitic DC resistance	50 GΩ
Node Z+ parasitic DC resistance	560 kΩ
Node Z- parasitic DC resistance	554 kΩ
Measurement condition: $V_{DD} = 0.6V$, $V_{SS} = - 0.6V$	

Tab. 2: Simulation results of the Bulk-driven CCII.

7. CONCLUSION

In this paper Bulk-driven CCII based on operational Transconductance Amplifier OTA is simulated using TSMC 0.18um CMOS technology with 0.6V power supply. Differential pair partially improves for power dissipation and terminal impedances but bandwidth reduces a when scaled down from 0.35um to 0.18um. CCII can be used as a voltage buffer and current buffer.

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