THD Investigation of Hybrid Cascaded Multilevel Inverter

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A B S T R A C T

Hybrid cascaded multilevel (HCML) inverter is a modification of the cascaded H-bridge (CHB) inverter, where this inverter has overcome the main drawback of the CHB inverter, which is the connection of a separate DC source in each H-bridge (cell). The solution was connecting one DC source in the first cell, and capacitors in the rest of the cells. Therefore, by controlling the switches of the inverter, the voltages of the capacitors can be regulated at a certain level and the inverter can generate an alternating voltage. In this paper, two cells and three cells HCML inverters have been simulated with Plecs software and modulated with phase shift- pulse width modulation strategy (PS-PWM). This modulation scheme was implemented with C language. The modulation program considers the load current and the voltages of the capacitors as feedbacks. The two inverters have been investigated in terms of the total harmonic distortion (THD) of the voltage and current waveforms. Therefore, the effect of the load sizes and cells number was addressed. Several significant results have been obtained from this study.

Keywords: CHB inverter, HCML Inverter, PS-PWM, THD.

1 Introduction

Cascaded multilevel inverter has become the solution for many renewable energy and motor drive applications due to the considerable advantages. The simplified topology (HCML inverter) has overcome the need to connect a separate DC source in every H-bridge. Therefore, it can suit a wider range of applications in the industry sector as the cost and the size of the inverter are reduced [1, 2, 3]. A growing body of literature has investigated different aspects of this significant inverter. However, one of the major areas of study is the total harmonic distortion in the output voltage and current waveforms generated by the inverter. As the THD contents affects the power quality delivered to the load [4, 5, 6]. In [5] selective harmonic elimination pulse with modulation was suggested to modulate the considered inverters, where the THD was decreased by 10%. In this paper, the methodology used to investigate the THD content in the output waveforms was based on simulation

processes. Two inverters with different cells number have been modeled and simulated with Plecs software. Thus, the number of cells and the load components (resistance and inductance) have been considered to explore their impacts on the THD of the output voltage and the load current. Based on that, several scenarios have been studied and compared with each other to understand the effect of the above factors on the THD content.

2 Connecting the Inverters

In order to examine the effect of the load and cells number on the total harmonic distortion content in the output waveforms of the hybrid cascaded multilevel inverter, Two cells and three cells HCML inverters have been built and simulated with Plecs software. The two cells inverter has two H-bridge cells. The first cell has four IGBTs switches connected to a 100 V DC source. The second cell has four IGBTs switches connected to a capacitor. Then the load was connected in parallel with the two cells as shown in Figure 1.

Furthermore, the three cell inverter has three H-bridge cells. The first cell has four IGBTs switches connected to a 100 V DC source. However, the second and the third cells have four IGBTs switches and connected to two capacitors as depicted in Figure 2. Therefore, the capacitors will replace the DC source in the second the third cells. Hence, by regulating the voltage of the capacitors at the level of 100 V, the inverters will generate alternating voltage with maximum voltage of 200V for two cells inverter with 5-level output voltage (200, 100, 0, -100, -200), whereas, 300V for three cells inverter with 7-level output voltage (300, 200, 100, 0, -100, -200, -300). Regulation process needs a modulation scheme that can provide the proper switching states for all switches. On the other hand, it needs to synthesis the right output voltage waveform with minimum THD.

For the two cells inverter, the capacitor value was 3.5mF, the load resistance was 0.5Ω, and the load inductance was 0.03H. However, for the three cells inverter, the two capacitors values were 4 mF, the load resistance was 1.11Ω, and the load inductance was 0.056H. The values of these parameters were selected based on the performance of the inverters, where these values offer the best operation and output waveforms.

3 Implementing PS-PWM Strategy

Phase Shift PWM (PS-PWM)) is tremendously common in the industrial applications particularly for CHB inverter. It is able to reduce the harmonics in the output, distributes the power equally between the H-bridges. PS-PWM was developed from the traditional sinusoidal PWM schemes especially for CHB inverters, where this scheme is based on multiple carriers (triangle wave carriers) compared with only one modulation signal. Each carrier is assigned to a certain H-bridge with a phase shift between the carriers.[7] Therefore, Phase shift-pulse width modulation was employed to modulate the two considered inverters. This modulation strategy was implemented in Plecs software by using C-script block. This block contains a programme written with C language, where the programme controls every

process in the inverter. However, the main tasks of the C code are to generate the modulation pulses for all the switches and balance the voltages of the capacitors. Maintaining the capacitors voltages requires measuring the voltages of the capacitors and load current and feed them back to the programme, so that the code can understand the case of the capacitors and take the decision whether to charge or discharge them depending on their voltages and the sign of the load current.

3.1 Modulating the Two Cells Inverter

The C-script block has 5 input signals, one modulation wave (sine wave) with 50 Hz and 0.8V amplitude. Two carrier waves (triangle waves) with 250 Hz and 1V amplitude, each carrier was assigned to one cell. Besides, the voltage of the capacitor was measured and fed back to the block as an input, and the load current was also measured and fed to the this block. Therefore, in order to maintain the capacitor voltage at a certain level, the C language programme has to read the values of the capacitor voltage and the load current, so that it can select the right switching states for the inverter's switches.

The two triangle carriers have a phase shift between them and that phase shift was calculated by using the following equation [8]:

Phase shift angle $\theta_k=[(k-1)/N]\times 180$ (1)

Where:

θ_k is the phase shift angle for each cell.
k is the individual number of the cell.
N is the total number of the cells.

Therefore, the calculated phase shift angles are $\theta_{HB1}= 0^{\circ}$, $\theta_{HB2}= 90^{\circ}$. On the other hand, to enter these angles into Plecs software, they must be changed to time base on the following equation [8]:

Phase shift time $T_k=[(k-1)/N]\times Ts/2$ (2)

Where:

T_k is the phase shift time for each cell.
k is the individual number of the cell.
N is the total number of the cells.
T_s is the carrier frequency inverse.

Therefore, the phase shift times between the carrier signals were obtained $T_{HB1}= 0$ sec, $T_{HB2}= 0.001$ sec. Moreover, C-script block has 8 outputs, one output for every switch in the two H-bridges as can be seen in Figure 1.

3.2 Modulating the Three Cells Inverter

As this inverter has three H-bridges, so it contains one capacitor in the second and one capacitor in the third cell. Therefore, the input signals of the C-script are 7. One sine wave (50Hz, 0.8V), three triangles waves (250Hz, 1V), two feedback voltage signals of both measured capacitors voltages and one feedback load current. The phase shift between the

three carriers are $\theta_{HB1}= 0^{\circ}$, $\theta_{HB2}= 60^{\circ}$, $\theta_{HB3}= 120^{\circ}$, while the phase shift times are $T_{HB1}= 0$ sec, $T_{HB2}= 0.000667$ sec, $T_{HB3}= 0.00133$ sec. For the outputs, there are 12 output signals exiting the C- script, one output for every switch in the three cells, as clearly depicted in Figure 2.

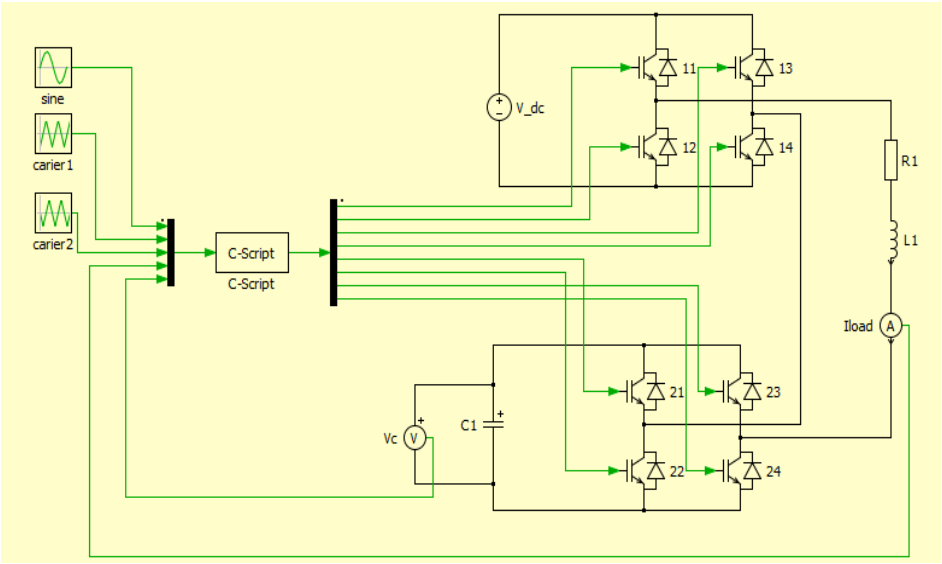

Figure 1: *Two cells HCML inverter circuit*

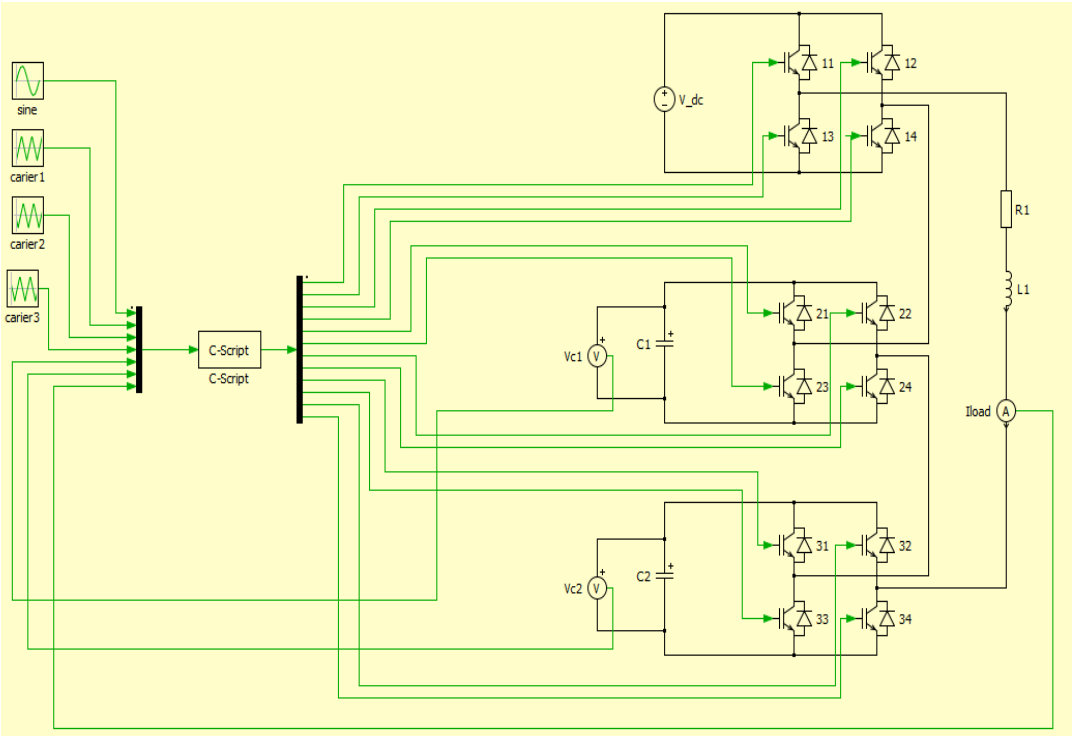

Figure 2: *Three cells HCML inverter circuit*

4 THD Study of the Two Inverters

In this section, the THD contents are studied in the output waveforms of the two inverters, where the inverters have been simulated under diverse resistance and inductance values. As one parameter was changing while the other was kept constant. At the same time, the THD readings of the output voltage and the load current were taken during the test at each time the parameter changes. Therefore, several THD readings have been recorded with each scenario.

4.1 THD Study under Load Resistance Effect

In this case, the impact of the load resistance on the THD was investigated. The resistance value was changed, while the other parameters of the inverter remained constant as mentioned above. Then, the THD readings were recorded as can be seen in Tables 1and 2.

Table 1: *THD readings when changing the load resistance (two cells inverter)*

R (Ω)	THD_v %	THD_I %
0.1	35.98	1.64
0.5	35.83	1.60
0.9	35.79	1.59
1.2	35.78	1.58
1.8	35.76	1.58
2.4	35.75	1.58
2.9	35.71	1.57

Table 2: *THD readings when changing the load resistance (three cells inverter)*

R (Ω)	THD_v %	THD_I %
0.1	25.22	2.07
0.5	25.13	0.99
0.9	24.97	0.87
1.11	24.95	0.86
1.15	24.82	0.85
1.20	24.64	0.81
1.25	24.59	0.77

Tables 1 and 2 present the results obtained from the simulation of the first scenario, where the effect of the load resistance was examined. It can be seen from the data that the THD of the voltage is larger than that of the current. This could be due to the switching frequency of the switches and due to the smoothing effect of the load inductance for the current.

Moreover, the THD of both the output voltage and the load current were relatively decreasing with increasing the resistance value. This may be attributed to the decreasing of the load current value, which in turn reducing the discharging current from the capacitor. The data shown in tables 1 and 2 were plotted in Figures 3 and 4 respectively. These two figures confirm that clear trend of decreasing of both THDs.

On the other hand, both THDs for three cells inverter are less than that of the two cells inverter. This was caused by the higher number of cells which led to synthesize more voltage steps (7 levels) in the output voltage in the three cell inverter, thus, the output voltage became closer to the sine wave. Consequently, as the cells number increases, the output voltage will have less THD.

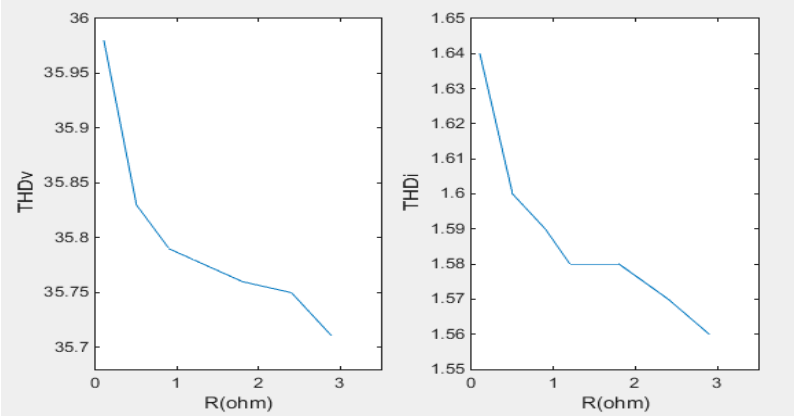

Figure 3: *THD readings when load resistance changing for two cells inverter*

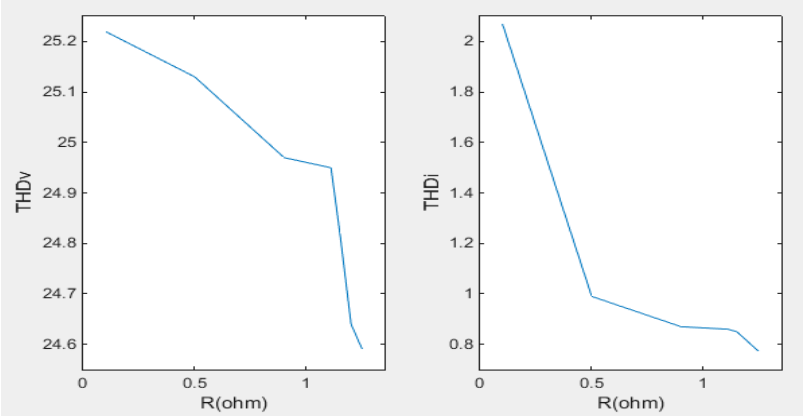

Figure 4: *THD readings when load resistance changing for three cells inverter*

4.2 THD Study under Load Inductance Effect

Another major factor that significantly affects the THD contents in the output waveforms, that element is the inductance of the load. Therefore, its impact was studied in this

simulation scenario. The inductance value was varied while the other parameters of the inverters kept untouched. Lower and higher inductance values than that values mentioned in section 2 were tested to recognise how the load inductance influences the THD contents of the HCML inverter. A number of readings have been taken according to these values as revealed in tables 3 and 4.

Table 3: *THD readings when changing the load inductance (two cells inverter)*

L (H)	THD_v %	THD_I %
0.01	35.83	1.62
0.03	35.84	1.58
0.05	35.86	1.56
0.07	35.89	1.51
0.09	35.93	1.47
0.10	36.00	1.42
0.15	35.71	1.57

Table 4: *THD readings when changing the load inductance (three cells inverter)*

L (H)	THD_v %	THD_I %
0.01	24.49	2.57
0.035	24.63	1.04
0.056	24.95	0.96
0.09	25.08	0.89
0.12	25.11	0.81
0.15	25.17	0.74
0.20	25.21	0.63

From the tables above, it is apparent that as the inductance value was increased, the THD of the output voltage was increasing too. This could be explained by the reducing power factor as the inductance increases, where the resistance value was remained constant. However, the THD of the load current was decreasing as the inductance value was increasing, which is due to the smoothing effect of the inductance for the current. Furthermore, the THD of both the voltage and the current in the case of three cell inverter is less than that of the two cells inverter. This is similar to the result of the resistance effect. Therefore, the cells number is a vital factor that can widely improve the THD contents in the voltage and current waveforms. As a result, the cells number is an independent factor from the resistance and inductance of the load, where as the number of cells increases, the THD content decreases. However, the cells number is limited by the size, cost and the modulating technique [9]. The data presented in table 3 and 4 were plotted as shown in Figure 5 and 6.

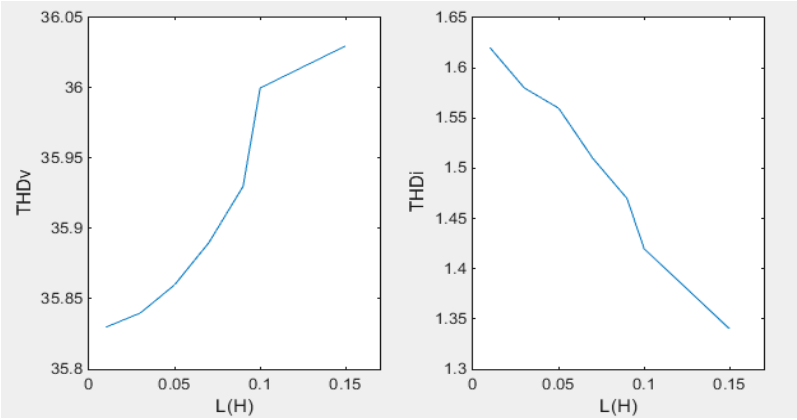

Figure 5: *THD readings when load inductance changing for two cells inverter*

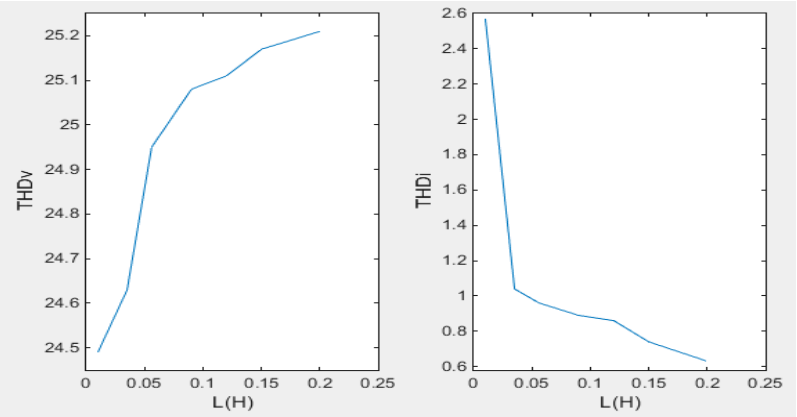

Figure 6: *THD readings when load inductance changing for three cells inverter*

5 Conclusions

A simulation investigation of the THD content was presented. Two cells and three cells hybrid cascaded multilevel inverters have successfully been modelled by Plecs software and simulated under various conditions. The resistance and inductance of the load have a serious impact on the THD of both the output voltage and current. For the resistance effect, it reduces the THD contents of both waveforms. However, the inductance has a different effect on both the voltage and the current. It deteriorates the voltage but improves the current. As a result, the design of the inverter should carefully consider the load, so that the inverter can operate at a wide range of loads with minimum THD contents. The cells number as an enhancing effect of both waveforms, but, it is a limited solution when it comes to the size and the cost of the inverter. Since the number of devices will be high.

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