Design of a Non-Isolated Solar PV Inverter for Household Applications

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ABSTRACT

Solar energy is taken into consideration as the promising alternative for the future energy demands to reduce carbon dioxide (CO_2) emissions from fossil fuel resources and to slow the depletion of limited energy resources. This paper presents a method on how to design a DC/AC inverter suitable for photovoltaic applications with focuses on minimizing the power losses and the cost.

Keywords: PV, H-inverter, MOSFET, DC-link and AC grid.

1 Introduction

The energy demand in Libya is steadily increasing and new types of energy sources must be found in order to cover the existing and future demands and to reduce the energy dependency on oil. Despite the challenges that face the General Electricity Company of Libya (GECOL) to build new fossil fuel plants, renewable energy opportunities are still strategically of high importance and must be adopted by the Libyan government.

One type of renewable energy sources is the photovoltaic (PV) cell, which converts sunlight to electrical current, without any form for mechanical or thermal interlink. PV cells are usually connected to make PV module, which generates a DC voltage and power depending on temperature and solar irradiation. PV modules can therefore not be connected directly to the grid but must be connected through an inverter. The two main tasks for the inverter are to capture the optimal PV module power, in order to harvest the most energy, and to inject a sinusoidal current into the grid.

The initial cost for a PV module is in the moment high compared with other sources. The price for a PV module, including inverter, cables and installation, is approximately 3.2$ per Watt [1]. This corresponds to a production-price of 0.06$ per kWh over a time period of 25 years (expected lifetime of PV boards), which cannot yet compete with the electricity supplied by GECOL which has a tariff of 0.02LD per kWh. However, it might be profitable for domestic use, since household and commercial electricity generators as an alternative to the public electricity often of poor quality with harmful impact to environment and increasing the price of diesel in the black market.

Moreover, PV power becomes more competitive by developing inexpensive and reliable inverters. This research has therefore focus on the field of inverter technologies, which is used to interface a PV module to the grid. This paper contains a combined analytical and simulation model of the PV inverter for household applications to determine the operating condition of the H-bridge inverter at no load and maximum power point and the parameters of power semiconductor devices, AC side inductance and DC-link capacitor. In this paper, PSIM software are used in circuit modelling and simulation.

2 Description of the H-bridge Inverter

Among various transformer-less topologies for PV application, the topology chosen due to power factor limitation is a PWM high power factor H-bridge where DC-AC conversion is required. The power circuit is presented in Fig. 1 for grid connected applications; the design values applied in this work are summarized in Table 1. V_{dc} represents solar panels output. Transistors M1-M4 are rated at full DC-link voltage which is in the range of 350-400V for regions such as Libya where RMS grid voltage is 230V. The switching frequency is intentionally chosen at 10kHz to push the first significant harmonic around $2f_{sw}$ seen in the voltage generated by the H-bridge, above audible noise which required to lower the environmental problems in household applications. In this study, the power rating of the converter is 2.5kW, which is a representative figure for residential PV application.

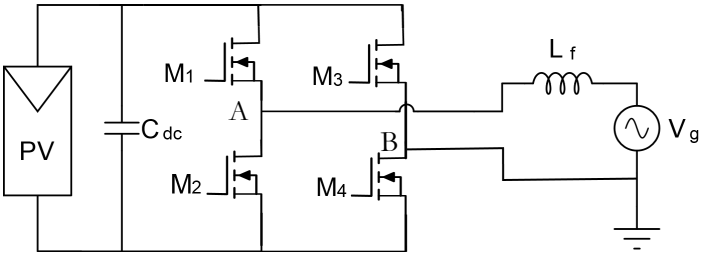


Figure 1: H-Bridge Inverter

Table 1: *Converter Parameters*

Parameter	Value
P_{max}	2.5kW
V_{dc}	400V
V_g	230Vrms/50Hz
f_{sw}	10kHz
PF	1

3 Photovoltaic Module – Inverter Interface

The specifications for the PV module interface correspond to the SPR-210 PV from SUNPOWER [2] are presented in Fig. 2. The voltage across the PV modules when it operates at the maximum power point is 40V at 1000W/m², and a cell temperature of 25˚C. In order

to avoid overmodulation in PWM scheme and to be able to control the grid current, it is necessary to choose the PV panel voltage at maximum power (smaller DC-link voltage) to be higher than the peak grid voltage plus the voltage drop across the semiconductors and the line side inductance.

The modulation index at full load is chosen to be $m_I = 0.9$ to avoid overmodulation.

$$V_{dc} \geq \sqrt{2}\ V_g/m_I = \sqrt{2}\ 230/0.9 = 361.4V$$

If we divide this voltage by the max power voltage of a panel (40V), number of 9.04 panels should be connected in series to supply the DC-link voltage. Practically the number of PV panels connected in series are chosen to be 10 PV panels. Therefore, the DC-link voltage at maximum power point is set equal to 400V.

$$V_{dc,MPP} = 10 \times 40 = 400V$$

However, in the worst case at no-load conditions (when maximum sun light falls on the PV panel) the maximum voltage that the DC-link of H-bridge inverter should withstand is:

$$V_{dc,max} = 10 \times 47.8 = 478V$$

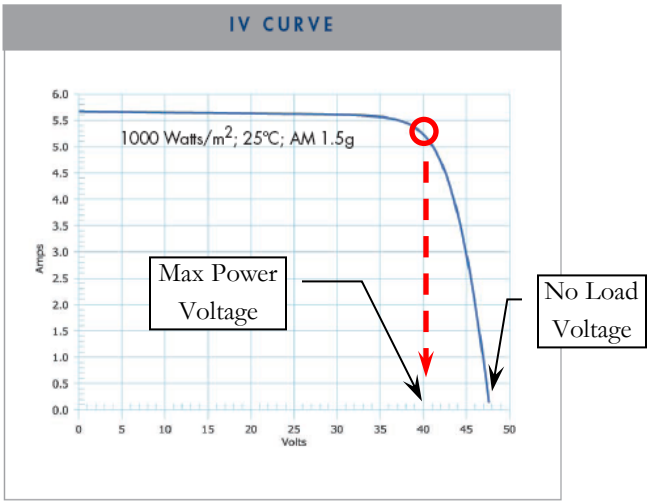
Thus, the inverter must withstand at least 478 V without being damaged. This condition of the H-bridge inverter at no load should be considered when selecting the DC-link capacitor rating.

SUNPOWER

ELECTRICAL CHARACTERISTICS AT STANDARD TEST CONDITIONS (STC)

STC is defined as: irradiance of 1000W/m², spectrum AM 1.5g and cell temperature of 25°C

Peak Power [1,2]	P_{max}	210W
Rated Voltage	V_{mp}	40.0V
Rated Current	I_{mp}	5.25A
Open Circuit Voltage	V_{oc}	47.8V
Short Circuit Current	I_{sc}	5.65A
Series Fuse Rating		15A
Maximum System Voltage		600V (UL)
		1000V (IEC)
Temperature Co-efficients	Power	-0.38%/°C



[1]Peak Power Tolerance: +/- 5%
[2]Power guaranteed for 25 years. See SunPower Limited Warranty for details.

Figure 2: Typical datasheet of a PV panel outlining the no-load and rated voltage/current and the V-I characteristic.

4 Selection of Power Semiconductor Devices

Since there are always safety coefficient that needs to be considered in the power transistor selection: the voltage de-rating $k_V=V_{stress}/V_{rating}$ (typically 0.6-0.7); and the current de-rating $k_I = I_{stress}/I_{rating}$ (typically 0.7-0.8).

The rated voltage of the power transistor devices used in H-bridge inverter with DC-link voltage of 400V is:

$$V_{rating} = V_{stress}/k_V = 400/0.7 = 571V \cong 600V$$

Here, 600V power MOSFETs are used for the two half-bridges. Use of external anti-parallel diodes is optional in the case of power MOSFETs, because of the presence of an intrinsic body diode. Using the body diode will decrease the high cost and the size of H-bridge power cell.

The maximum sinusoidal current that can be processed by these devices assuming a ratio of k_I between the current rating of the switch and the peak value of the RMS current is:

$$I_{rating} = I_{stress}/k_I = 10.9 \times \sqrt{2}/0.8 = 19.2A \cong 20A$$

The selection of the power MOSFET is a trade-off between cost and power losses. The selected MOSFET transistor (IPA60R160P7XKSA1) has specifications of 600V blocking voltage, 20A continuous current, 0.12Ω on-state resistance, and housed in a TO-220 encapsulation. The MOSFET body diode has forward voltage of 0.9V and low reverse recovery charge of 1.7μC [3]. MOSFETs for the DC/AC inverter are selected among the CoolMOS type from Infineon, because they have very good properties in terms of cost versus power losses.

The total conduction losses P_{cond} in the MOSFET at full generation is equal to 7.03W, and the switching losses P_{sw} found equal to 6.14W. The heat-sink thermal resistance is calculated equal to 0.66 ˚C/W considered the reference heat-sink temperature equal to 60˚C for some industrial applications, i.e. PV inverters, and ambient temperature chosen equal to 25˚C.

The device junction temperature by considering the device total power loss and ambient temperature is computed to 111.6˚C for ambient temperature of 45˚C during warm times in summer. This is, however, still seen safe for the power device since the device junction can withstand 150˚C without being damaged (from datasheet) [3]

5 Selection of the AC inductance

The output filter of grid-connected inverter is to smooth the output ripple injected to the grid caused by high switching frequency. The filter AC inductance of H-Bridge inverter is determined by selecting the most relevant frequency domain voltage harmonics generated by the H-bridge inverter. As shown in Fig. 3, the FFT of the voltages generated by each of the H-bridge inverter leg with reference to the DC-link mid-point (top two plots) and the result

in the FFT of the line-to-line voltage generated by the H-bridge inverter (bottom), revealing the cancelation of the switching frequency harmonic around 10 kHz and the doubling of the fundamental voltage. The results in Fig. 3 shows that the most severe switching harmonic is placed at 20kHz with peak voltage of 100V.

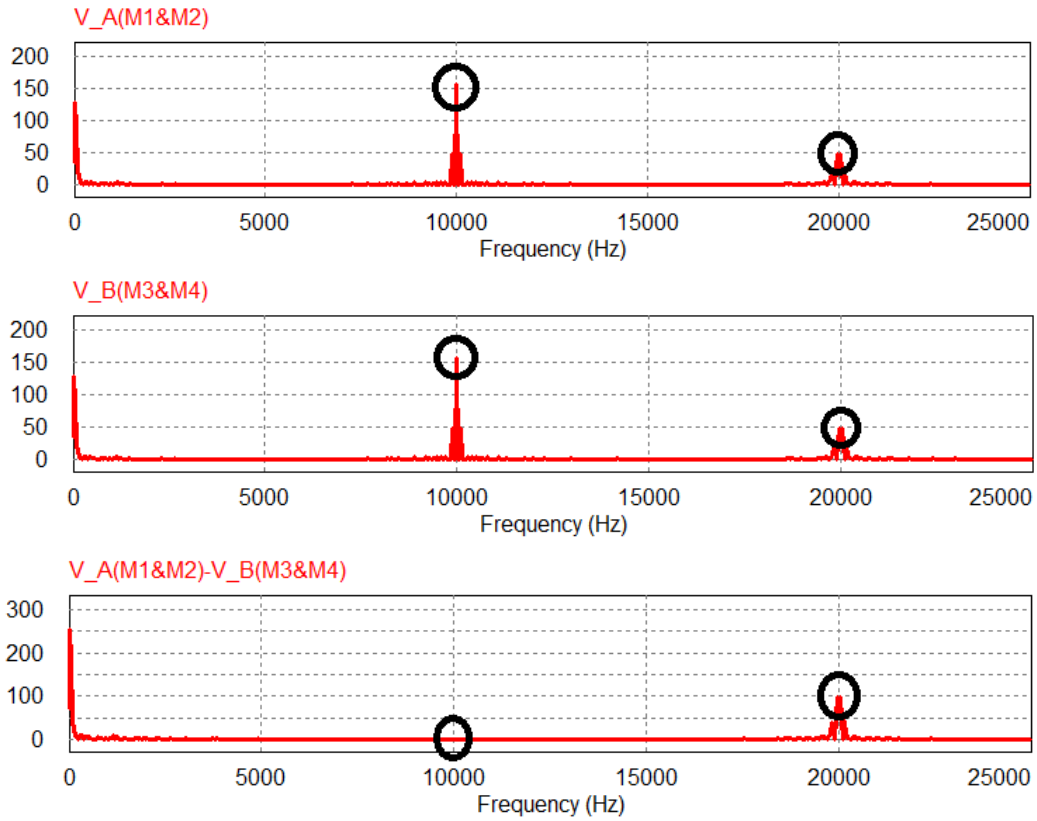


Figure 3: The FFT of the voltages generated by each of the H-bridge inverter legs and the line-to-line voltage (bottom).

According to EN61000-3-2-A standard for current harmonics, any harmonics must be limited below 2 % of the fundamental current (here 218mA) [4].

$$L_{AC,min} = \frac{V_{h-pk}}{2\pi . f_h . \sqrt{2} . \Delta I_h} = \frac{100}{2\pi . 20 . 10^3 . \sqrt{2} . 218 . 10^{-3}} = 2.6mH$$

Magnetic material selection is the first step for inductor design. In comparison, ferrite can achieve low loss at high switching frequency, on the other hand ferrite has low saturation flux density. Although amorphous is characterized by high flux density, but it is prone to high core losses at high switching frequency [5]. Therefore, for this topology and at this power level, ferrite core made from 3C92 material with low losses at high switching frequency, low cost and relatively high saturation (540mT) is the preferred choice in solar inverters [6].

In sizing the inductor, the winding area (Aw) is calculated first based on the current density of 500A/cm², for Ip=10.9×$\sqrt{2}$=15.4A, Aw=0.0308cm². The core permeance AL (nH/turn²) is determined using $A_L = L/N^2$, and then locating the value on the core selector table; the first core size located above the calculated value is the smallest core size that can be used in the design. Ferrite core E71/33/32-3C92-G500 with 50 turns was designed with the target to provide inductance of 2.6mH [6].

The core loss in the inductor P_{fe} is estimated equal to 10.2W from the core loss curves normally provided by the manufacturer in the datasheet, while the power loss in the winding is calculated equal to 5.3W and given by:

$$P_{cu} = \rho \frac{N.MLT}{A_w} I^2 = 1.72 \times 10^{-8} \frac{50 \times 160 \times 10^{-3}}{0.0308 \times 10^{-4}} 10.9^2 = 5.3W$$

where *MLT* is Mean-Length-per-Turn of the core, *N* is the number of turns of the winding (copper) and *I* is RMS value of winding current.

The total power loss in the inductor is found:

$$P_{ind} = P_{fe} + P_{cu} = 10.2 + 5.3 = 15.5W$$

6 Determining the DC-link Capacitor

The DC-link capacitor in H-bridge inverter topologies is used to absorb not only the high switching frequency components of the PWM converter current but also for the low frequency current components showing twice mains frequency (i.e. 100Hz for 50Hz mains frequency) due to the pulsating power flow seen in single phase topologies. The DC-link capacitor is distributed into two stages, which are the input bulk capacitors and the stage of high frequency decoupling filters. The input bulk capacitors are based on electrolytic capacitor technology which are good for low frequency ripple. However, high frequency decoupling capacitors based on film technology are responsible for high frequency current ripple.

At full power, the maximum 100Hz current ripple will then be determined [7]:

$$I_{C(rms)} = \frac{I_{dc}}{\sqrt{2}} = \frac{6.25}{\sqrt{2}} = 4.4A@100Hz$$

where I_{dc} is the ripple free DC output current and equal to I_{dc} =P_{dc}/V_{dc}=2500/400=6.25A.

The size of DC-link capacitor can be determined by imposing the power into the DC-link and the peak-peak DC-link voltage ripple which is limited to say 2% of the DC-link voltage (or smaller), otherwise an oscillation in the extracted power from the PV panel will occurred due to the voltage ripple in the dc-link.

$$C_{dc,min} = \frac{P_{dc}}{2\omega . V_{dc} . \Delta V_{dc(peak)}} = \frac{2500}{200\pi . 400.4} = 2.49mF$$

The selection is made to a standard electrolytic capacitor (ALS70A332MF) of a 3.3mF and ESR=77mOhm and rated at 500V to allow for some over voltages to withstand at no-load voltage condition, without damaging the capacitor.

A final check is performed to ensure that the capacitors can handle the 100Hz current ripple. From the datasheet, this capacitor can handle up to 12.3A@100Hz, which means that the 4.4A@100Hz which is the actual current ripple stresses in the DC-link capacitor can be easily handled.

The DC-link capacitor bank power loss at full power level:

$$P_{C-loss} = ESR.I^2_{100Hz-RMS} = 0.077.(4.4)^2 = 1.5W$$

In addition, two film capacitors with 14µF, 630V and ESR=1mOhm each (B32676G6146K) are connected in parallel giving total capacitance of 28µF with negligible power loss.. They are mounted very close to the half bridges of H-bridge inverter to create a low impedance path for the HF ripple current, since the electrolytic capacitors are good only up to some kHz.

Fig.4 shows the waveform of the DC-link voltage. The result is a 396-404 V peak-to-peak voltage ripple of 8V, which is exactly the imposed value (4V peak) in the design stage for the DC-link capacitance.

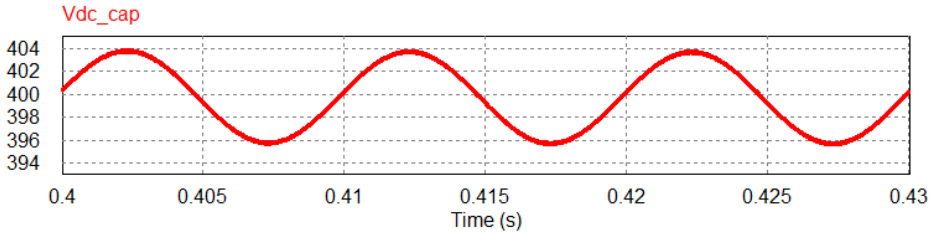


Figure 4: The voltage across the DC-link capacitors.

7 Estimation of the converter losses

The total loss P_{total} of the H-Bridge inverter can be defined as a sum of conduction P_{cond} and switching P_{sw} losses in all MOSFET devices, DC-link capacitor loss $P_{C\text{-}loss}$ and inductor loss P_{ind}.

$$P_{total} = 4P_{sw} + 4P_{cond} + P_{C-loss} + P_{ind}$$

$$P_{total} = 4 \times 6.14\text{W} + 4 \times 7.03\text{W} + 1.5\text{W} + 25.7\text{W}=79.9\text{W}$$

$$\eta = 1 - \frac{P_{circuit}}{Pin} = 1 - \frac{79.9}{2500} = 96.8\%$$

The efficiency of the inverter operating at 10kHz is estimated equal to 96.8% at full power which is satisfactory for this topology and at this power level.

8 Conclusions

In this paper, a combined analytical and simulation model to design a DC-AC inverter for PV applications was developed. Focus has been on determining the operating condition of the H-bridge inverter at no load and maximum power point based on the PV panel characteristics. In addition, the parameters of semiconductor devices, AC side inductance and DC-link capacitor are selected to obtain a low-cost solution with high efficiency.

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