مجلة التربوي

مجلة علمية محكمة تصدر عن

كلية التربية الخمس

جامعة المرقب

العدد الخامس

يوليو 2014م

هيئة التحرير

بحوث العدد

- الأثر الدلالي لحروف العطف على الأحكام الفقهية .
- قراءة نقدية في الأبيات الشعرية المنسوبة لكثير عزة، تحقيق ودراسة في نقد النقد "قديما وحديثا" .
- مظاهر من النقد الأدبي في طور نشأته .
- بعض العوامل المؤثرة في اتجاهات طلاب جامعة الجبل الغربي نحو النشاط الرياضي .
- Analysis and Comparison of Estimated Carry Adder with other Adder Designs
- The Importance of Listening Comprehension In Language Teaching and Learning

الافتتاحية

الحمد لله على توفيقه، والشكر له على دوام عطائه، يصدر - وبفضل منه تعالى - العدد الخامس (يوليو 2014م) من مجلتكم "مجلة التربوي" التي تحاول أن تخدم الباحثين والقراء، وتسعى لأن تحظى برضاهم عنها، وليس من عجب أن يشعر أعضاء هيئة التحرير بالسعادة والفخر وهم يقدمون للقارئ العزيز هذا العدد الجديد الذي أثراه الباحثون بأبحاثهم القيمة التي تفيد القارئ وفي شتى مجالات المعرفة .

ومع إطلالة هذا العدد، العدد الخامس من مجلتكم "مجلة التربوي" نجدد العهد مع قراء المجلة الكرام بأن تكون دوما ملتزمة بنشر الجديد والمفيد والهادف من الأبحاث العلمية التربوية، وتعتذر أشد الاعتذار لأصحاب البحوث والقراء عن تأخر إصدار العدد الرابع عن موعده المقرر له؛ وذلك راجع إلى صعوبات خارجة عن نطاق هيئة التحرير، كما نعتذر عن تأخر هذا العدد الذي ابتنى تأخره على تأخر العدد الذي قبله، ولكننا - وبإذن الله - نطمح إلى أن يصدر كل عدد في موعده المحدد له – إن شاء الله تعالى - وبشيء من جهد أعضاء هيئة التحرير التي لا تستغني أبدا عن مساندتكم ومؤازرتكم جميعا بحاثا ومقيّمين وقراء نصل إلى الهدف المنشود الذي تبتغيه المجلة .

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Abstract

A large number of adders have been proposed, but adding fast adder using low area and power is still challenging. In 2001 a new 32-bit asynchronous adder has been introduced (32-bit ESTC adder)[1], which used the estimation theory to improve the speed of addition time. This paper presents a design and implementation of the necessary control circuit for 32-bit ESTC adder and compares it's performance and area with other previous adder designs. It has been seen through analysis of the design and operation with previous work that the Estimated Carry Adder provides a compromise between high speed, high area cost adders (carry lookahead adder) and slow, low area adders (carry ripple adder). Comparison with well-known conventional adders demonstrates that 32-bit ESTC adder dramatically achieve speeds and/or area advantages over previously adder circuits.

Introduction

Adders are of fundamental importance devices of digital systems, and the performance of any digital systems or processors is very influenced by the speed of their adders. The time required to perform an addition (computation time) in an adder is the time required for propagating the carries (carry propagation time) in addition stages, plus one more delay to compute the sum (*S*) bits. The computation time of an adder is sensitive to the size of the numbers to be added. The larger the number of bits in an operand, the slower the addition process becomes.

Therefore, to increase the speed of a digital systems, the main focus of research into adder structures is mainly concerned with optimising the speed of processing whilst minimising the hardware space required by the adder.

Many fast adders for high speed have been introduced last few years [2, 3, 4, 5]. However, always high-speed adders are necessary for high performance in digital applications. Thus, research into improving the performance of digital adders is an important field.

One of these fast adders A 32-bit Estimated carry adder (ESTC) was first introduced in [1], and it has been shown that by using a single probabilistic carry prediction a 32-bit adder can be

constructed in which for the majority of additions will operate as 16-bit parallel adder. Consequently, this reduces the overall average time delay, and the amount of hardware overhead for the adder. Then a new approach for Estimated carry adder was designed [6] which extended the estimation theory for the carry in which correct prediction could be increased and as a result further performance benefits for a 32-bit ESTCA adder can be achieved over the current method by using more carries for prediction.

This paper presents the design and implementation of the control circuitry for the additional prediction inputs for the new approach, and to analyze and compare the most interesting known adders with this a new approach.

Implementing the Control Circuit for a 32-bit ESTC Adder

The adder circuit operates as two N/2-bit adders concurrently, and this is described as a short delay. On the other hand, in the case of incorrect estimation the circuit waits for the LS adder to finish and then propagates the true carry, and subsequently the MS adder continues with the addition. In this situation the addition time is similar to the delay time of a full N-bit adder, plus the time needed to detect the state and apply the correct value. This is described as a long delay. The configuration of a carry control circuit using two

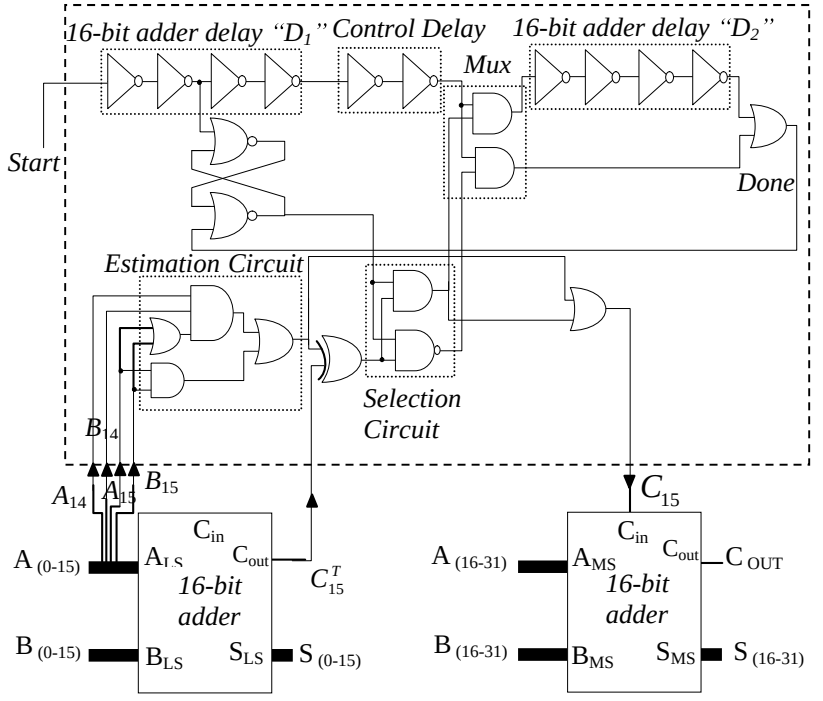

Figure 1: Schematic of the control circuit for a 32-bit estimated carry adder using two carries for prediction

carries has been employed to design a new completion control circuit for a 32-bit ESTC adder. This circuit will generate the correct carry out from the LS adder to the MS adder, and determines whether a short or long delay should be used, as shown in Figure 1.

Initially, all signals are set to zero and then a pulse signal is applied to the start input. The start pulse sets the RS flip-flop, which is then held in the set state until a signal is returned when the addition is complete. At this point the flip-flop is reset and a new set of data can be applied to the adder. This prevents spurious carry states from being generated prior to the evaluation of the next carry state during the next addition cycle. Of course, the done signal shouldn't indicate completion even momentarily before an addition is complete. If an input changes after an addition has been completed, the completion signal should immediately go off and remain off until the next new sum is completed. The start pulse places a high signal on the output of the second NOR gate which feeds the selection circuit (the NAND and AND gates). These two gates control the two delay lines; specifically they determine which delay should be used for a specific set of inputs.

When the carry is estimated correctly, the carry out from the LS adder propagates to the MS adder using a short delay. However, if the estimated carry is different from the true one, then the true carry must be applied to the MS adder. This will occur after the LS adder has completed the addition, and in such a case the time needed will be the same as a 32-bit full adder plus a small delay incurred in detecting the state and applying the correct value.

Consequently, during a short delay the done signal is set after a delay of D_1, Mux., and OR gate; whereas in the case of a long delay, the result is available after a delay of D_1, Mux, D_2 and OR gate.

The control circuit was implemented and simulated for functional behaviour by using Aldec Active-HDL™ Software, and the simulation shows that the practical results are in line with the theory.

The Results

The new approach of a 32-bit ESTC adder design has examined and compared with other commonly used adder architectures in terms of addition speed, area requirements, and delay-area product. This section presents the optimisation results obtained. In addition, graphical representations of the area and speed tradeoffs that characterise the different adders are presented.

Simulations have been performed using PSPICE with parameters from a 0.125 μm CMOS technology [1, 7], and the results achieved agreed with the theory. Simulations were performed for three different types of adder with two different structures: the 4-bit ripple adder and the 4-bit carry lookahead adder. The reasons for choosing these types are that:

(i) The ripple carry adder is the simplest and most commonly used adder.

(ii) The carry lookahead adder is one of the fastest adders used for the addition of two numbers.

(iii) The carry select adder chosen for the reason that the design in this research uses the same idea for carry select but reduce its area by removing one of the MS adders and the multiplexer completely, instead using control circuits to generate the carry out from the LS adder to the MS adder.

Typically, adder performance is characterised in terms of area and speed. Thus, this section focuses on evaluating the delay time and the hardware cost of the circuits, comparing them with other designs. The comparisons were carried out by analysing the area requirements and the maximum operational speed, since this provides a convenient way to compare the advantages and trade-offs of the different designs. The comparison is divided into two subsections; firstly the ESTC adder using a single carry for prediction is compared with the different types. Secondly, the ESTC adder using multiple carries is compared with other adder designs.

Table 1: Comparison of delays and transistor numbers for simulated 32-bit adders

Adder Structure	*Delay, (ps)*	*Area (Transistors No.)*
32-bit CLA/CLA	100	3425[8]
32-bit CSLA/CLA	121	2832
32-bit CSLA/RA	584	2424
32-bit ESTCA/CLA	166	1756
32-bit RA/CLA	203	1680
32-bit ESTCA/RA	627	1530
32-bit RA /RA	1064	1408

RA/RA: ripple adder with ripple elements
RA/CLA: ripple adder with carry lookahead elements
CSLA/RA: carry select adder with ripple elements
CSLA/CLA: carry select adder with carry lookahead elements
CLA/CLA: carry lookahead adder with carry lookahead elements
ESTCA/RA: estimated carry adder with ripple elements
ESTCA/CLA: estimated carry adder with carry lookahead elements

ESTC Adder using Single Carry for Prediction

Results obtained for a 32-bit ESTC adder using a single carry for prediction are listed in Table 1, and are also presented graphically in Figure 2.

It can be seen from Table 1 that for the adders based on the 4-bit ripple adder, the ripple adder (RA/RA) uses the smallest area but is very slow compared to the carry select adder (CSLA/RA), which is faster but uses a larger hardware area. The estimated carry adder

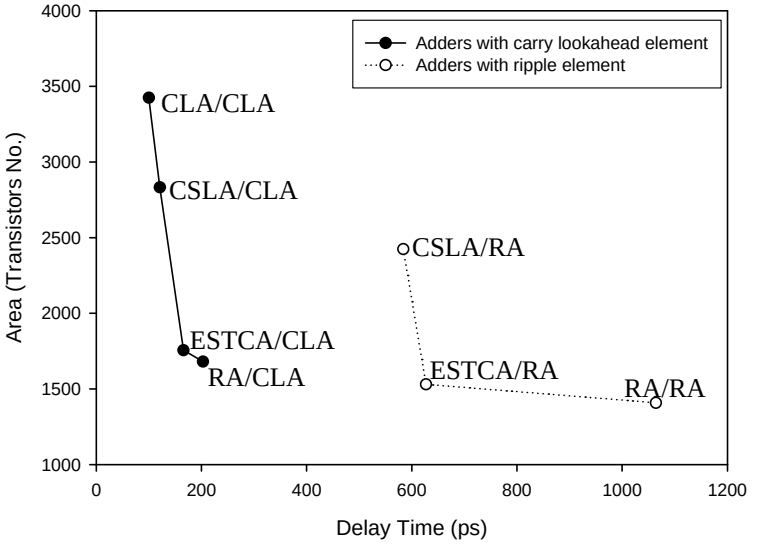

Figure 2: Simulation results for 32-bit adders

(ESTCA/RA) offers a significant speed advantage of 41% over the RA/RA for only an 8.7% increase in hardware area. In addition, the ESTCA/RA is only 7% slower than the CSLA/RA but it uses 37% less area. On the other hand, as expected, the adders based on the 4-bit carry lookahead adder show speed advantages over those using ripple adders because the carry calculations are made in parallel.

However, they use more hardware compared with those using ripple adders because the computations in a carry lookahead adder are performed in parallel, which requires a larger number of gates, and which also uses a larger area. The RA/CLA is the slowest of this group; however it is still faster than the CSLA/RA and uses less area. The CLA/CLA is the fastest, but uses the greatest area. The CLA/CLA is 40% faster than the ESTCA/CLA, but uses nearly double the area required for ESTCA/CLA (95%). Also the CSLA/CLA is 27% faster than the ESTCA/CLA, but uses 61% more area. The ESTCA/CLA is 18% faster than the RA/CLA, for an increase of only 4% in area.

ESTC Adder using Multiple Carry for Prediction

This subsection presents the simulation results for multiple estimated carry adder. In addition, graphical curves presenting the tradeoffs in terms of delay and area are presented.

In the beginning, a comparison of the multiple estimated carry adders using different numbers of carries for prediction was performed. Then comparisons between this adder design and other relevant adders were undertaken.

Table 2: Comparison of 32-bit ESTC adders using multiple carries for prediction

Adder Structure	*Carries used for Prediction*	*Delay (ps)*	*Area (Transistor No.)*
32-bit ESTC/RA	Single Carry(C_{15})	627	1530
	Two Carries(C_{14})	571	1546
	Three Carries(C_{13})	544	1556
	Four Carries(C_{12})	533	1568
	Five Carries(C_{11})	531	1582
32-bit ESTC/CLA	Single Carry(C_{15})	166	1756
	Two Carries(C_{14})	151	1772
	Three Carries(C_{13})	144	1782
	Four Carries(C_{12})	141	1794
	Five Carries(C_{11})	140	1808

The values of delays and transistor numbers for all configurations were computed for the ESTC adder and are listed in Table 2. The results are organised separately for the ESTC/RA and ESTC/CLA adders. Since the speed advantage gained after C_{11} is not practical (because it is limited by the complexity), the comparisons were not carried out for more than five carries. Furthermore, graphical curves presenting the tradeoffs in terms of delay and area are shown in Figures 3 and 4.

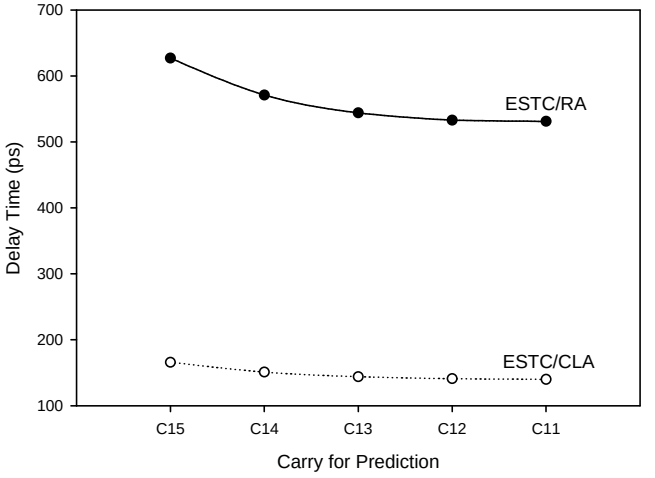

Figure 0: Delay vs. multiple carries used for prediction

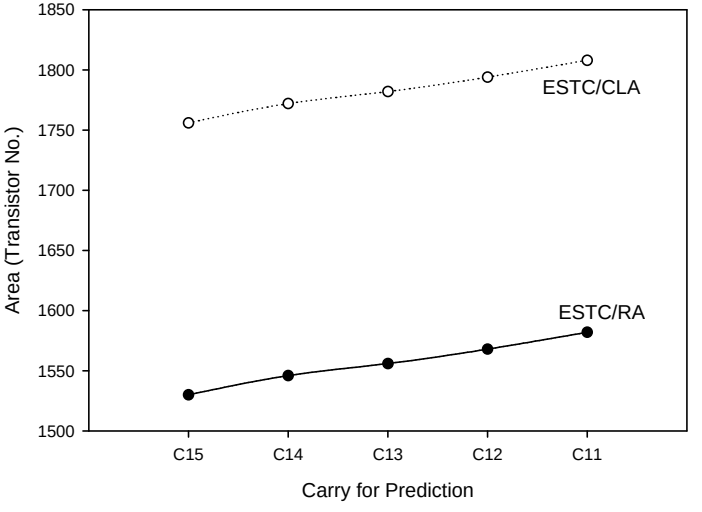

Figure 4: Area vs. multiple carries used for prediction

Table 0: Comparison of multiple ESTC adder with other adders

Adder Structure		*Delay (ps)*	*Area (Transistors No.)*	*Delay-Area Product*
32-bit CLA/CLA		100	3425	342500
32-bit CSLA/RA		584	2424	1415616
32-bit CSLA/CLA		121	2832	342672
32-bit RA /RA		1064	1408	1498112
32-bit RA/CLA		203	1680	341040
	Carries used for Prediction			
32-bit ESTC/RA	Single Carry	627	1530	959310
	Two Carries	571	1546	882550
	Three Carries	544	1556	845842
	Four Carries	533	1568	835509
	Five Carries	531	1582	839647
32-bit ESTC/CLA	Single Carry	166	1756	291496
	Two Carries	151	1772	267413
	Three Carries	144	1782	255824
	Four Carries	141	1794	252147
	Five Carries	140	1808	252758

Delay-area product is computed by multiplying logic complexity (area) and time complexity (delay)

Figure 3 shows that the delay of the ESTCA decreases as more carries are used for prediction. It is noticeable how, as the number of carries used for prediction increases, the delay of the ESTC/RA adder decreases much faster compared to that of the ESTC/CLA adder. This was expected because of the linear increase in the delay of the RCA versus the logarithmic increase in the delay for the CLA.

On the other hand, the increase in area requirements for this adder shown in Figure 4 is very small when the number of the carries used for prediction increases. This is because few additional logic gates are needed for the control circuit as more carries are used. The increase in area requirements is linear when the numbers of carries used for prediction are increased.

The results of performance comparisons for the multiple ESTC with other designs in Tables 3 show that there are considerable performance advantages to be made when a new carry is introduced for prediction; however, this takes a considerable amount of hardware and the circuit becomes more complex and more expensive in terms of silicon area. This means that the estimated carry adder will be competitive in speed and/or size when compared with other adder designs. These results can be explained as follows:

1. Multiple ESTC vs. Adders with RCA Elements

For the adders based on the ripple adder, the RA/RA still has the smallest area but is very slow compared to others. However, the comparison of multiple the ESTC/RA with other designs shows significant speed advantages. For example, it is offers speed advantage of 46.3% over the RA/RA for only 9.8% of increasing in

hardware area when two carries are used for prediction, By using three carries for prediction, the ESTC/RA is 48.9% faster and uses just 10.5% more area, and it is 49.9% faster and uses just 11.4% more area when four carries used for prediction. Additionally, by using five carries, it is 50.1% faster than RA/RA and it uses just 12.4% more area. Furthermore, by comparing ESTC/RA with CSL/RA, it is 2.25% faster but it uses 36% less area, 6.9% faster and uses 35.8% less area, 8.8% faster and uses 35.3% less area, and 9.1% faster and it uses 34.7% less area when 2, 3, 4, and 5 carries used for prediction respectively.

2. Multiple ESTC vs. Adders with CLA Elements

Comparing the multiple ESTCA/CLA with the adders that are built from CLA blocks demonstrate that the CLA/CLA is still the fastest but at the greatest expense of area. The CLA/CLA is 31% faster than ESTCA/CLA using three carries for estimation but uses 92% more area. In addition comparing the ESTCA with RA/CLA shows that it is 25.7% faster for only 5.5% more area when two carries are used, 29.3% faster for only 6.1% more area when three carries are used, and 30.8% faster for only 6.8% more area when four carries are used. Also speed advantage of 31.1% can be gained over the RA/CLA for only 7.6% of increasing in area when five carries are used for prediction.

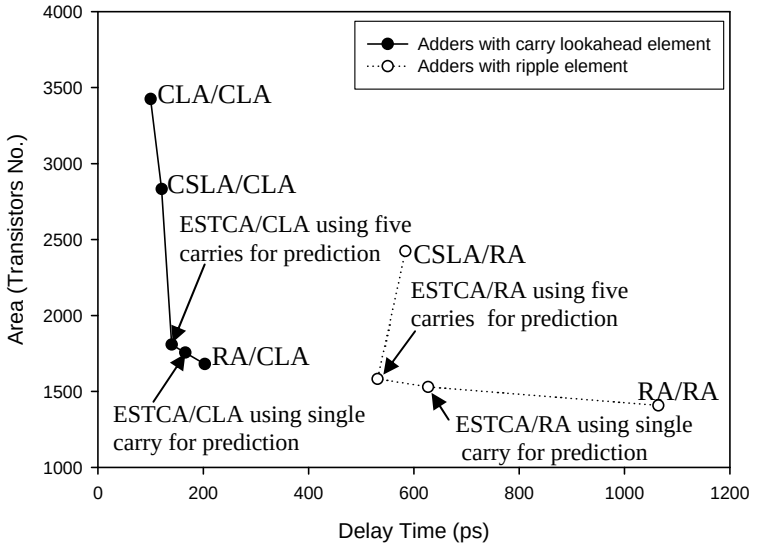

Figure 5: Results of 32-bit adders compared with multiple ESTC adder using five carries for prediction

Also comparing ESTC/CLA with the CSL/CLA shows that CSL/CLA is 19.8% faster but uses 59.7% more area. Furthermore, CSL/CLA is 15.7% faster but uses 59.9% more area, 13.9% faster but uses 57.9% more area, and 13.4% faster but uses 56.6% more area when 2, 3, 4, and 5 carries used for prediction respectively.

Table 3 gives a clear overview of the tradeoffs obtained for the multiple ESTCA using different numbers of carries compared to other designs, and Figure 5 represents the simulation results of 32-bit adders compared with multiple ESTC adder using five carries for prediction.

Table 3 shows that the for the adders based on RA, and when two, three, four, and five carries are used for prediction, the multiple ESTC design offers savings of 41.1%, 43.5%, 44.2%, and 44% over RA/RA respectively, and savings of 37.7%, 40.2%, 41%, and 40.7% over CSLA/RA respectively. Similarly, the results for the adders based on the carry lookahead scheme, CLA, show that the multiple ESTC adder gives savings over the RA/CLA of: 21.6% in the case of using two carries, 25% when using three carries, 26.1% when using four carries, and 25.9% when using five carries. The ESTC/CLA gives savings over the CSL/CLA adder of 22% using two carries, 25.3% using three carries, 26.4% using four carries, and 26.2% using five carries. The ESTC/CLA gives savings over the CLA/CLA of 22%, 25%, 26.1%, and 26.2% when two, three, four, and five carries respectively are used for prediction. The graph in Figure 6 gives a clear overview of the delay-area products obtained.

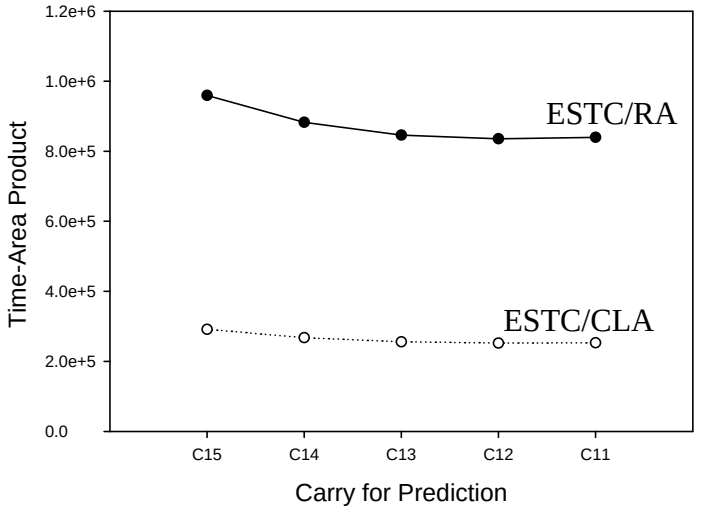

Figure 6: Delay-area product comparison as more and more carries are used for prediction

Conclusion

In this paper qualitative and quantitative comparisons of adder structures and designs have been carried out. Particularly, it presents comparisons of the 32-bit ESTC adder vs. other adder designs, where simulations have been performed for three different types of adder with two different structures. Simulation results for the ESTC adder, and graphical curves presenting the tradeoffs between this design and other common digital arithmetic blocks such as RCA, CLA, and CSLA adders were obtained in this work.

In additional, the ESTC adder using multiple carries for prediction significantly reduces the delay and offers major improvements in speed over other adders while remaining compact. Thus the ESTC adder speeds up addition time and is considered a competitive with other more commonly used adders when used for high performance applications.

The overall results demonstrate that the ESTC adder is simple, fast and suitable for implementation using VLSI technology. Also the results suggest that there are substantial performance gains to be made by adopting the approach and methodology using multiple carries for prediction for the asynchronous ESTC adder.

References

1. Wallace W. F., Dlay S., and Hinton O., 'Probabilistic Carry Estimate for Improved Asynchronous Adder Performance', IEE Proceeding of Comput. Digit. Tech., Vol. 148, No. 6, 2001, pp. 221-226.
2. Chih-Jen Fang, Chung-Hsun Huang, Jinn-Shyan Wang, Ching-Wei Yeh, 'Fast and compact dynamic ripple carry adder design', IEEE Asia-Pacific Conference on ASIC, USA, 2002, pp. 25-8.

3. Nagendra C., Irwin M. and Owens R., 'Area-time-power trade-offs in parallel adders', IEEE Transaction on Circuits and Systems-II: Analog and Digital Signal Proc., Vol. 43, No. 10, 1996, pp. 689-702.
4. Kyung-Nam Han, Sang-Wook Han, Euisik Yoon, 'A new adder scheme with reduced P, G signal generations using redundant binary number system', Proc. of IEEE International Symposium on Circuits and Systems, part Vol. 5, Switzerland, 2000, pp. 633-6.
5. Hashemian R., 'A new Design for High-speed and High-density Carry Select Adders', Proceeding of the 43rd IEEE Midwest Symposium on Circuits and Systems, Vol. 3, 2000, pp.1300-3.
6. E. M. Ashmila, S. S. Dlay, O. R. Hinton, "Multiple Carries Prediction to Enhance the Performance of a 32-bit Estimated Carry Adder", Fourth international symposium on communication systems, networks and digital signal processing (CSNDSP), United Kingdom, 20-22 July 2004, pp 617-621 (626-629).
7. William Frederick Wallace, Design and Analysis of Probabilistic Carry Adder, thesis at University of Newcastle upon Tyne, August 2002.

8. Wang C.C., Tseng Y.L., Lee P.M, Lee R.C., and Huang C.J., 'A 1.25 GHz 32-bit tree-structured carry lookahead adder using modified ANT logic', IEEE Trans. on Circuits and Systems-I : Fundamental Theory and Applications, vol. 50, No. 9, 2003, pp. 1208-1216.
9. Zhao Bing, Hei Yong, Qiu Yulin., 'An asynchronous add-compare-select design in CMOS VLSI', 5th International Conference on ASIC, IEEE. Part Vol.2, USA, 2003, pp.1277-80.
10. Mark A. F. and Tienyo P., 'Performance Comparison of Asynchronous Adders', IEEE Proceedings of International Symposium on Advanced Research in Asynchronous Circuits and Systems, ASYNC-94, Salt Lake City, Utah, Nov. 1994, pp. 117-125.
11. E. M. Ashmila, O. O. Aldawibi, "Extension of Estimation Theory to improvement of Asynchronous Adders's Performance", Rawafed Al-Marefa Journal, Arts and Science Faculty, Tarhona, Zaytouna University, Vol. 1 June 2013, pp 1-22.

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